Notice of Allowability	Application No.	Applicant(s)
	10/705,887	WANG ET AL.
	Examiner	Art Unit
	Prabodh M. Dharia	2629
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308. 1. This communication is responsive to 01-17-2007.		
2. The allowed claim(s) is/are <u>4-19</u> .		
3.		
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. Notice of Informal Page 1. Interview Summary Paper No./Mail Date 7. Examiner's Amendm 8. Examiner's Stateme 9. Other	(PTO-413), e

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1. Status: Please all the replies and correspondence should be addressed to Examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 01-17-2007 under amendments, which have been placed of record in the file. Claims 4-19 are pending in this action. Applicant has cancelled claims 1-3.

Response to Amendment

2. Applicant has amended objected dependent claim 4 by adding independent claim 1 limitations. Applicant has cancelled claims 1-3; Claims 4-19 are pending. Claims 5-19 were allowed. Applicant's arguments, see Remark, filed 01-17-2007, with respect to Claims 4-19 regarding "A driving circuit of a liquid crystal display device including a timing controller, a source driver and a low color scale driving circuit, the timing controller outputting a polarityinverting signal, a first digital signal, a second digital signal, a third digital signal and a fourth digital signal, the low color scale driving circuit generating a first analog signal, a second analog signal, a third analog signal and a fourth analog signal and comprising: a plurality of buffers. receiving the polarity-inverting signal, the first digital signal, the second digital signal, the third digital signal and the fourth digital signal; and a plurality of sets of transistors which comprise a first set of transistors, a second set of transistors, a third set of transistors, and a forth set of transistors, respectively coupled to an output terminal of the buffers for respectively outputting the first, second, third and fourth analog signal" have been fully considered, searched and are persuasive as they do overcome prior art rejection; which puts application number 10705887 in condition for allowance.

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3. Applicant amended claim 4 has no new matters added to the claims. The amended claims do have support in specification.

Allowable Subject Matter

- 4. Claims 4-19 are allowed.
- 5. The following is an examiner's statement of reasons for allowance:
- 1. Applicant's argument filed on 01-17-2007are convincing. As argued by applicant in remarks under claim rejection page 6, paragraphs 6-11, and page 7, paragraphs 1-4 the prior art of Saito et al. (2002/0140711 A1) in view of Naito (US 2002/0126106 A1) and Poor (US 2004/0131279 A1) fails to recite or disclose the uniquely distinct features represented by underlined bold claim below;

A driving circuit of a liquid crystal display device including a timing controller, a source driver and a low color scale driving circuit, the timing controller outputting a polarity-inverting signal, a first digital signal, a second digital signal, a third digital signal and a fourth digital signal, the low color scale driving circuit generating a first analog signal, a second analog signal, a third analog signal and a fourth analog signal and comprising: a plurality of buffers, receiving the polarity-inverting signal, the first digital signal, the second digital signal, the third digital signal and the fourth digital signal; and a plurality of sets of transistors which comprise a first set of transistors, a second set of transistors, a third set of transistors, and a forth set of transistors, respectively coupled to

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an output terminal of the buffers for respectively outputting the first, second, third and fourth analog signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance.

Conclusion

- 6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.
- 7. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
- 8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

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January 25, 2007

BIPIN SHALWALA SUPERVISORY PATENT EXAMINER

TOWNOLOGY CENTER 2600